AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 1, line 5 of the originally filed application, with the following amended paragraph:

The present application is related to U.S. Patent Application Serial No. 09/841,079 "Extended Range Image Processing For Electro-Optical Systems", ~~Serial No. _____ (Attorney Docket No. 017750-575),~~ and to U.S. Patent Application Serial No. 09/841,081 ~~entitled~~ "Dynamic Range Compression", ~~Serial No. _____ (Attorney Docket No. 017750-700),~~ both filed even date herewith, the disclosures of which are incorporated herein by reference in their entirety.

Please replace paragraph [0030] of the originally filed application with the following amended paragraph:

[0030] Various aspects of the invention will now be described in connection with a number of exemplary embodiments. To facilitate an understanding of the invention, many aspects of the invention are described in terms of actions to be performed by a processor unit, a processor, and/or a field programmable gate array (FPGA) device. It will be recognized that in each of the embodiments, the various actions could be performed by elements of a computer system. Further, it will be recognized that in each of the embodiments, the various actions could be performed by specialized circuits (e.g., discrete logic gates interconnected to perform a specialized function), by program instructions being executed by one or more processors, or by a combination of both. Moreover, the invention can additionally be considered to be embodied entirely within any form of computer readable carrier such as solid-state memory, magnetic disk, optical disk or modulated carrier wave

(such as radio frequency, audio frequency or optical frequency modulated carrier waves) containing an appropriate set of computer instructions that would cause a processor to carry out the techniques described herein. Further, the invention can additionally be considered to be embodied within an appropriate set of computer instructions that can be downloaded via a network connection to cause a processor to carry out the techniques described herein. Thus, the various aspects of the invention can be embodied in many different forms, and all such forms are contemplated to be within the scope of the invention. For each of the various aspects of the invention, any such form of embodiment can be referred to herein as "logic configured to" perform a described action, or alternatively as "logic that" performs a described action.

Please replace paragraph [0031] of the originally filed application with the following amended paragraph:

[0031] FIG. 1 illustrates a block diagram of an apparatus 100 for gathering and processing imagery, such as infrared (IR) imagery, according to an exemplary aspect of the present invention. The apparatus 100 could, for example, be incorporated into a forward looking infrared (FLIR) camera system such as that described in commonly-assigned U.S. Patent ~~Application No. 09/463,410 entitled~~ No. 6,359,681 "Combined Laser/FLIR Optics System", the disclosure of which is hereby incorporated by reference in its entirety.

Please replace paragraph [0061] of the originally filed application with the following amended paragraph:

[0061] An exemplary level routine 800 pertaining to generating a preliminary level correction factor for each detector channel consistent with the SBNUC routine 700 will now be described with reference to FIGS. 7 and 8. As indicated at block 702 of FIG. 7 and at step 804 of FIG. 8, a two-dimensional frame of input scene data is directed to a vertical high-pass filter (HP1) to generate a frame high-passed data (HP data) (e.g., first high-passed data). The HP1 filter is carried out by choosing a given pixel to be a central pixel with two vertically adjacent pixels (one above and one below), multiplying the three pixel values by appropriate scale factors, and subtracting from the value of the central pixel the sum of the pixel values above and below; the resulting value is assigned to be the corresponding pixel value for the frame of HP data. A pixel of one frame "corresponds" to a pixel of another frame if the pixels have the same column and row location. The HP1 filter is accordingly a convolution filter and can be carried out in binary form with a (-.25, .5, -.25) kernel (the negative signs indicate subtraction as described above). This kernel is the same as a true high-pass filter with the coefficients of (-1/3, +2/3, -1/3) * d1 where the factor d1=¾ is a damping factor. The d1=¾ damping factor has the beneficial effect of damping the filtered values to enhance stability of the SBNUC routine and also provides for ease of implementation in a binary hardware design because the damped filter provides for divide-by-two and divide-by-four arithmetic operations. Generally, the damping factor d1 can range from approximately 0.5-0.95; d1=0.75 has been found to be advantageous. The HP1 high-pass filter (and other high-pass

filters disclosed herein) can be applied to edge pixels using techniques well known in the art such as mirroring pixels about the edge, folding pixels about the edge, replicating edge pixels, and padding edge pixels with zeros, as disclosed, for example, in above-incorporated U.S. Patent Application entitled "Dynamic Range Compression", Serial No. 09/841,081 ~~Serial No. _____ (Attorney Docket No. 017750-700)~~.